CS-GIIB Integrated Inverter

Technical Brief

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CS-GIIB Manual Revision History

Card Revision 1.0:

Release 1.0	-	Initial Release
Release 1.1	-	Typographical
Release 1.2		Updated Layout

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1.0 Overview of the CS-GIIB Inverter System

The CS-GIIB is a flexible, low voltage, 4-phase leg integrated inverter controller that has been designed for applications requiring a single simple inverter platform. The board is designed to operate with a plug-in processor card, as a standalone inverter.

The board consists of 6 major sections:

- 8 off complementary isolated gate driver PWM outputs, with common fault interrupt
- Isolated RS-232 serial interface
- 16 off conditioned analog inputs
- 4 off DAC outputs
- LCD interface / Keypad interface / Digital I/O
- Switch-mode power supply to generate all on-card supplies

The system can be operated with the gate drivers supplying up to 30kVA and 600Vdc inverter power stages. For even larger external power stage devices, the gate driver output capacity can be increased to an 8A peak using a transistor totem pole pair on the driver output.

The CS-GIIB Integrated Inverter measures 345mm x 200mm.

On-card facilities include:

- Serial Interface (Isolated RS232)
- Quadrature Position Encoder input with Index
- High speed clocked serial peripheral interface
- 4096 bit serial ROM
- Dual Temperature Sensors (digital)
- Multiple off-card digital I/O ports
- On-card DIP switches and status LEDs
- 6 off AC current inputs
- 3 off differential AC voltage inputs
- 4 off differential DC voltage inputs
- 2 off potentiometer analog inputs
- 1 off general analog input
- 4 off DAC outputs
- 1 off 4x5-way keypad decoder
- LCD interface, with contrast
- 2 off MOSFET switch output
- 8 off complementary isolated gate driver PWM outputs, with common fault interrupt
- 8 bit MINI bus interface (INTEL iSBX compatible),
- +24V isolated field supply

Figure 1-1 shows a functional block diagram of the CS-GIIB Integrated Inverter, illustrating all major sections.

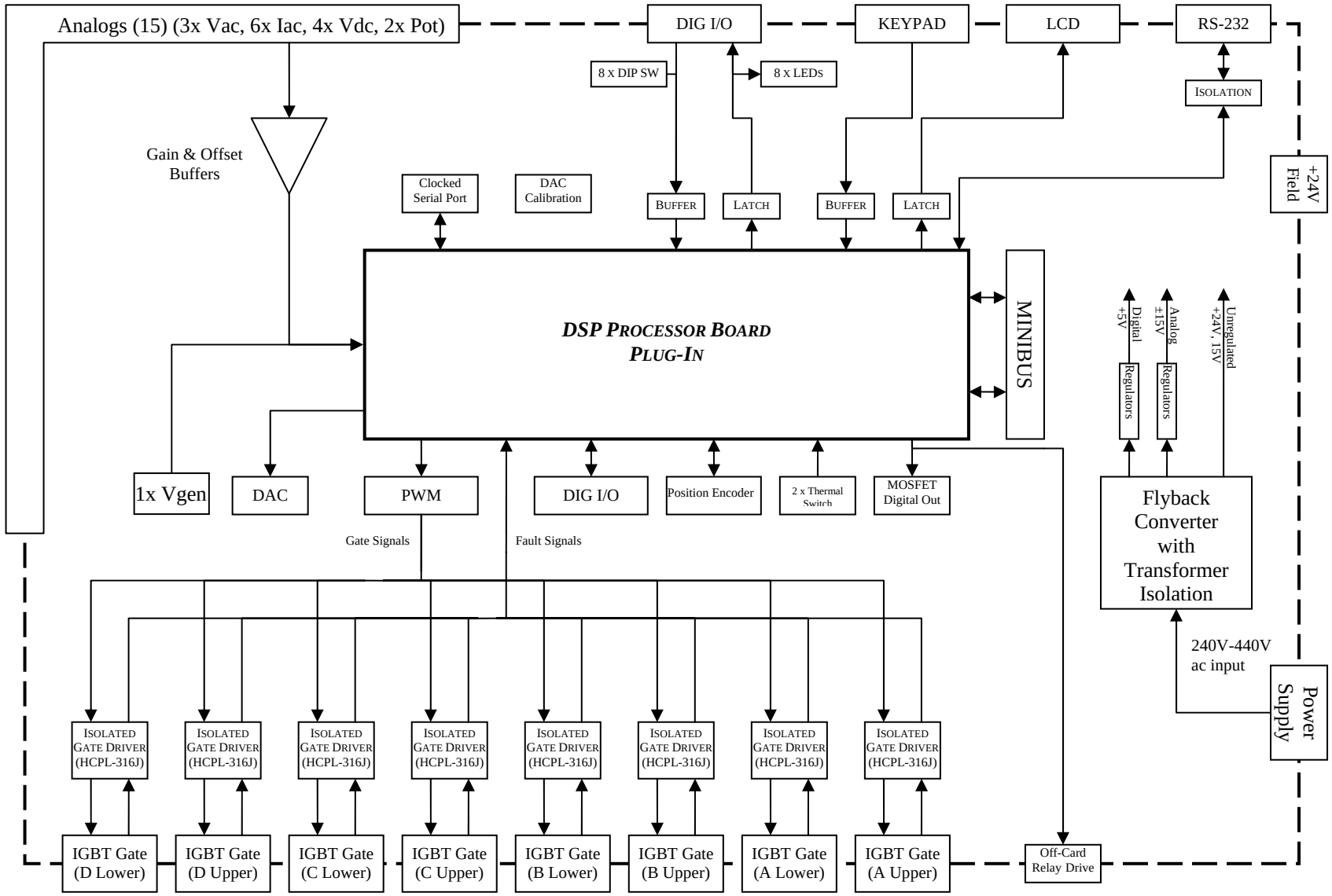


Figure 1-1: Functional Diagram of CS-GIIB Integrated Inverter Board

1.1 Digital I/O

The CS-GIIB card supports 32 bits of digital I/O, configured as two banks of 16 bits each. One bank of 16 I/O bits, Bank 1, supports local I/O, and interfaces to 8 off LEDs and 8 off DIP switches. The second 16 bit I/O bank, Bank 2, has no local I/O facilities, but has shared functionality with the position encoder, zero crossing and sample and hold circuitry. Each I/O port can also be accessed via an IDC header connector (normal ribbon cable type connector). Bank 1 has a 26-way IDC header, with Digital Ground, +5V and +12V connections available for use by external interface circuitry and is accessed as a Mini Bus peripheral port by the DSP controller. Bank 2 is accessed directly from the MiniDSP plug-in interface via a 20-way IDC header, with Digital Ground and +5V connections brought out for use by external interface circuitry.

1.2 Analog Inputs

The analog inputs to the CS-GIIB are conditioned as 6 off AC currents, 3 off AC voltages, 4 off DC voltages, 2 off potentiometer inputs and 1 off general ±10V input. These inputs then interface to the CS-MiniDSP as ± 10V analog inputs.

The six AC current inputs are entirely independent, although they are notionally arranged as two sets of three phase inputs. All AC current inputs require burden resistors to be fitted to the card, selected so that the full-scale voltage developed across each resistor ranges between ±5V to suit LEM transducers. Standoffs are provided on-card for ease of mounting these resistors. If required, capacitors can be added in parallel with the burden resistors to reduce unwanted high frequency noise. Note that for CT transducers, the front end gain of the current amplifiers may need to be adjusted to allow a reduced burden voltage for this type of measurement.

Currents I1 and I2 include a sample and hold capability on the CS-GIIB. This capability, together with the inbuilt sample and hold provided with the analog inputs of the DSP controller, allows measurements for currents I1, I2 and I3 without time skew. There is a common overcurrent detection circuit for this set of AC current inputs, with the trip level determined by a resistor mounted on standoffs.

Currents I4, I5 and I6 have separate grounds provided on their input connectors so that each current input can be connected using individual twisted pair wires from a CT input. These current inputs have no sample and hold or overcurrent detection capability.

The 3 analog AC voltage inputs are measured as differential with respect to a separate fourth input. This allows a complete set of three phase voltages to be measured with respect to floating neutral points. The AC voltage inputs have a default input voltage range of ±450V peak. This can be reduced by mounting gain resistors onto standoffs on the PCB.

Voltages Vac1 and Vac2 include a sample and hold. This capability, together with the inbuilt sample and hold provided with the analog inputs of the DSP controller, allows measurements for voltages Vac1, Vac2 and Vac3 without time skew. Input voltage Vac1 has a zero-crossing detect circuit, which is arranged to drive a DSP capture digital input by insertion of a jumper link.

The 4 off DC voltage inputs have a default input voltage range of 510V. This can be reduced by mounting gain resistors onto standoffs on the PCB or alternatively increased by the addition of off-card series resistance. Each DC voltage input is a differential high impedance circuit, which measures the DC voltage between two floating rails. Two of the DC inputs connect to a common overvoltage detection circuit, with the trip level determined by a resistor mounted on standoffs.

The 2 off potentiometer inputs and the 1 off general analog input accept inputs in the range of ±10V. The potentiometer inputs can be link selected to use either on-card trimpots or off-card external potentiometers. A ± 10V nominal reference voltage is available at the off-card potentiometer connectors to energise the external potentiometers, with a maximum total current of 2mA. The general input has ±15V and AGND available on its connector.

1.3 Analog Outputs

There are 4 off analog outputs on the CS-GIIB that are produced from dual 8 bit multiplying DACs. Each DAC output is conditioned to produce a bipolar output (±10V). Each channel can be independently calibrated and all DAC outputs are fed to a single 10-way IDC header. The DACs are accessed as Mini Bus peripheral ports by the DSP controller.

1.4 Gate Drive Interface

The CS-GIIB supports 8 PWM channel outputs generated by the plug-in DSP processor board, and converts them into 8 isolated gate driver outputs through HCPL-316J gate driver chips. Isolated supplies are generated on-card for each gate drive circuit. The gate driver signals are available on external connectors.

Gate fault signals from the eight HCPL-316J gate driver chips are linked together and connected to the PDPINT* interrupt. This interrupt provides a hardware interrupt to the DSP immediately upon detection of a fault, which disables the PWM signals using internal hardware logic within the DSP.

If a gate drive current greater than 2A is required (the HCPL-316J has a maximum 2A output limit), a totem pole option can be added to each gate drive circuit to drive larger off-card switching devices (up to 8A peak).

A 16-way IDC header is also provided to enable the logic level gate signals to be connected to an alternative source or output. To drive the gate signals from an off-card source (ie not through the DSP controller) the plug-in DSP controller must have any output buffered signals disabled.

1.5 Communications

The CS-GIIB integrated inverter board supports an isolated RS-232 serial interface, and a non-isolated TTL high-speed synchronous serial peripheral interface.

The RS-232 serial interfaces between the TTL-level MiniDSP UART interface and the off-card differential RS-232 signals. There are HCPL-2211 high-speed optocouplers used to isolate the UART receive and transmit signals and an ESD protected RS-232 transceiver enables a conventional PC serial port to interface directly to the circuit board. An NMF0505 or NKE0505 DC-DC converter provides the isolated supply for this serial port.

The TTL high-speed synchronous serial peripheral interface can be used to communicate for clocked serial communications to other controllers. The interface is buffered to support either master or slave protocol, selected by software.

1.6 On-card memory

The CS-GIIB integrated inverter board has no direct on-card memory, as it is designed to operate only with a processor board plug-in to the pin strip headers provided. The preferred controller board is the CS-MiniDSP, which supports 64k x 16 bits each of on-card Program RAM and Data RAM, although any compatible controller board is acceptable.

The CS-GIIB integrated inverter board does support 256 x 16 bits of non-volatile serial ROM. This ROM is accessed using the high-speed clocked serial peripheral interface in Master Mode.

1.7 Position Encoder

The position encoder interface accepts quadrature encoded pulses from a relative position encoder system, and uses these pulses to update a 16 or 32 bit position counter (as selected by software) within the DSP. The phase A and Phase B signals interface to the DSP using shared digital I/O bits on the Digital I/O Bank 2 Connector.

A separate index pulse input can be used to generate an interrupt to reset this counter for initialisation purposes. This signal interfaces to the DSP through the Digital I/O Bank 2 Connector.

The encoder input signals are at 5V TTL levels, diode clamped to avoid damage caused by input overvoltages. A +12V supply is also provided at the encoder input connector for use by the external encoder circuitry.

1.8 Keyboard Interface

The keypad input is arranged to accept a 9 wire, 4x5 matrix keypad input through a 20 way IDC header, which interfaces to a 74C923 keypad decoder. This encoder is accessed as a Mini Bus peripheral port by the DSP controller.

1.9 LCD Interface

The LCD interface is arranged to directly suit all 1 and 2 line Handok or Optrex character type LCD display modules. The interface connects to the LCD display through a 16 way IDC header connector. The interface signals are an 8 bit latched data byte, and four latched control bits which are toggled by the DSP to generate the LCD display control signals. All interface signals are TTL.

The LCD interface also provides a –12V adjustable contrast supply, and a +5V LED backlight supply controlled by a transistor switch.

The LCD interface data and control bit latches are accessed as Mini Bus peripheral ports by the CS-MiniDSP controller.

1.10 MOSFET Driven Digital Outputs

The CS-GIIB board has two MOSFET driven latched digital outputs. Each output is capable of switching +12V 200mA supply controlled by a Power FET and is designed to direct drive a 12V relay coil. The free-wheel diode is present on the CS-GIIB board. These digital outputs are accessed on a Mini Bus peripheral port by the DSP controller.

1.11 Power Supply

The standard CS-GIIB integrated inverter board has an on-card switch mode power supply that accepts an input voltage in the range of 90V – 270V AC or 130V – 370V DC. The SMPS generates all necessary on-card supplies as well as an isolated +24V field supply for off-card use.

2.0 Specifications

2.1 Analog Inputs

Number of Channels	16
Plug-In Interface to header	**X21** (which corresponds to J4 on the CS-MiniDSP)

2.1.1 AC Current Inputs

Definition	3 off twisted pair 3-wire connections and 3 off twisted pair 4-wire connections providing conditioned AC current inputs compatible with CT's and LEM's. Burden resistors (**R18** – **R23**) and low pass filter capacitors (**C14** – **C19**) are required to suit input current requirements
Input Voltage Range	±5V maximum peak (set by burden resistor for required current)
Burden Resistor	AXIAL0.4 component mounted on-card and sized according to input voltage range and maximum required current input AC current input impedance is 5k0 without the burden resistor
Overcurrent Protection	Overcurrent linkable interrupt to PDPINT* (LK8) for first three current inputs I1, I2 and I3. Trigger current determined by resistor selection (R148)
Sample and Hold	Sample and Hold circuitry fitted for currents I1 and I2. S&H control signal supplied from CS-MiniDSP as digital output bit R4*, I/O Bank 2 (**X30**) through link **LK10**
LEM Supply	± 15V 100mA supply available to support LEMs. (**X5** – **X10**)
Dynamic Response	Cut-off frequency >150kHz
PCB Connections	3 off 3 terminal plug-in PCB Mounting Terminal Block with ±15V. (**X8** –**X10**) 3 off 4 terminal plug-in PCB Mounting Terminal Block with ±15V and AGND. (**X5** – **X7**)

2.1.2 AC Voltage Inputs

Definition	3 off AC voltage differential analog inputs, arranged as two sets of 3 inputs. Each set measures voltage with respect to a separate fourth floating common
Input Voltage Range	±450 Vac maximum peak Lower range available with placement of scaling resistors (**R2**, **R27**, **R44**, **R75**) Higher range available through placement of off-card series resistors
Sample and Hold	Sample and Hold circuitry fitted for voltages Vac1 and Vac2. S&H control signal supplied from DSP as digital output bit R4*, I/O Bank 2 (**X30**) through link **LK10**
Input Protection	High input impedance, 450kΩ in default configuration
Dynamic Response	Cut-off frequency > 450kHz
PCB Connections	7 pin plug-in PCB Mounting Terminal Block (**X14**)

2.1.3 DC Voltage Input

Definition	4 off DC voltage differential analog inputs
Input Voltage Range	0 – 510Vdc Lower range can be achieved by changing surface mount resistors (see circuit schematic) Higher range can be achieved through the addition of off-card series resistors
Input Protection	High input impedance, 510kΩ in default configuration
Overvoltage Protection	Direct interrupt to DSP for VDC3 and VDC4. Overvoltage linkable interrupt to PDPINT* (**LK7**). Trigger voltage determined by resistor selection (**R149**)
Dynamic Response	Cut-off frequency >450kHz
PCB Connections	2 pin plug-in PCB Mounting Terminal Block (**X20**, **X24**, **X25**, **X28**)

2.1.4 Potentiometer Analog Inputs

Definition	2 off analog potentiometer inputs
Voltage Range	-10V to +10V
Options	Links provided to enable the use of the on-card pots (**LK3**, **LK4**)
PCB Connections	3 pin plug-in PCB Mounting Terminal Block, with +10V, signal & -10V (**X12**, **X13**)

2.1.5 General Analog Input

Definition	1 off General Analog input
Voltage Range	-10V to +10V
PCB Connections	4 pin MASCON Connector, with +15V, signal, -15V and AGND (**X33**)

2.2 Analog Outputs

Definition	4 off 8-Bit Buffered Multiplying DACs with output signal conditioning
Voltage Range	$-\frac{128}{128}\times 10V = -10V$ to $\frac{127}{128}\times 10V = 9.92V$
Gain Trim Resistors	**R37** – **R40**
PCB Connection	10 pin shrouded IDC header, with output signals, and interleaved AGND (**X32**)
Plug-in Interface to header	Accessed via Mini Bus, Port W4, W5, W6, W7

2.3 Mini Bus Interface

Mini Bus Description	8 data bits, 3 address bits, 3 I/O select lines, control signals (similar to Intel iSBX microbus)
Mini Bus I/O Address Space	24 I/O ports on Mini Bus, accessible as 3 banks of 8 addressable ports. Uses I/O space addresses: 0x0C000 – 0x0C017
PCB Connections	36-way non-shrouded DIL header (**X22**)
Plug-In Interface to header	**X23** (which corresponds to J1 on the CS-MiniDSP)

2.4 Digital Inputs

2.4.1 TTL Level Inputs

Definition		2 banks of 8 bit TTL digital inputs Note: each bank is on a separate IDC connector, which is shared with TTL digital outputs. +5V (DVCC) and DGND made available on connector for external use
Maximum input voltage		5V DC
Minimum input voltage		0V DC
PCB Connection	Bank 1	26 pin shrouded IDC header, with signals, logical ground, +5V supply and unregulated +12V supply (**X4**)
	Bank 2	20 pin shrouded IDC header, with signals, logical ground and a +5V supply (**X30**)
Plug-in Interface to header	Bank 1	Accessed via Mini Bus, Port R0 (Base Address + 00h)
	Bank2	**X26** (which corresponds to J2 on the CS-MiniDSP)
See High Speed CMOS Logic Data book for further details		

2.4.2 Position Encoder Digital Inputs

Definition	1 pair of quadrature encoded pulses defining relative position change 1 index pulse
Maximum Input Voltage	5V DC
Minimum Input Voltage	0V DC
Dynamic Response	Up to 4 MHz pulse trains, limited by DSP internal counter timing for quadrature encoded inputs and interrupt response time for index pulse
Input Protection	Diode clamped to DGND and DVCC, Schmitt trigger buffered input, 1k0 input impedance
PCB Connection	10 pin shrouded IDC header, with signals, logical ground and a +12V unisolated supply (**X29**)
Plug-in Interface to header	**X26** and **X18** (which corresponds to J2 and J6 on the CS-MiniDSP)

2.4.3 Keypad Input

Definition	9 wire 4x5 matrix decoded keypad input at TTL input levels
PCB Connection	20 pin shrouded IDC header, with signals, logical ground and a +5V supply (**X3**)
Plug-in Interface to header	Accessed via Mini Bus, Port R1

2.5 Digital Outputs

2.5.1 TTL Level Outputs

Definition		2 banks of 8 bit TTL digital outputs Note: each bank is on a separate IDC connector, which is shared with TTL digital inputs, see section 2.4.1. +5V (DVCC) and DGND made available on connector for external use
Digital outputs rated at		±35mA per bit, ABSOLUTE MAXIMUM
Typical digital high output voltage @ 10mA source		4.34V
Typical digital low output voltage @ 10mA sink		0.33V
PCB Connection	Bank 1	26 pin shrouded IDC header, with signals, logical ground, +5V supply and unregulated +12V supply (**X4**)
	Bank 2	20 pin shrouded IDC header, with signals, logical ground and a +5V supply (**X30**)
Plug-in Interface to header	Bank 1	Accessed via Mini Bus, Port W1 (Base Address + 01h)
	Bank2	**X26** (which corresponds to J2 on the CS-MiniDSP)
Note: Output voltage specified for +5V VCC See High Speed CMOS Logic Data book for further details		

2.5.2 MOSFET Outputs

Definition	2 off MOSFET switched outputs
I_{source}	1.2mA @12V, through 10kΩ pull up resistor
I_{sink}	200mA nominal 1A absolute maximum
Switch Configuration	Single pole, normally open. Direct connection to ground
Isolation	No isolation provided
PCB Connections	3-way Molex connector (**X34**) – DIGOUT1 3-way plug-in PCB Mounting Terminal Block (**X36**) – DIGOUT2
Plug-in Interface to header	Accessed via Mini Bus, Port W2 Bit 1 and Port W2 Bit 2

2.5.3 LCD Display Interface

Definition	16 pin LCD display output consisting of 8 bits of strobed output data, 2 bits of latched digital output (to be used to set up LCD display module control signals) one write signal, contrast and backlight enable
Contrast Control	Variable display brightness voltage, +5V to -10V
Digital outputs rated at	±35mA per bit, ABSOLUTE MAXIMUM
PCB Connections	16 pin shrouded IDC header (**X2**)
Plug-in Interface to header	Accessed via Mini Bus, Port W0 (Data) and Port W2 (Control)

2.6 PWM Gate Drive Interface

2.6.1 Isolated Gate Drives

Definition	8 PWM Outputs
PWM Outputs	8 PWM outputs consisting of – Each output is driven from an isolated +17V/-12V supply that is generated on-card
Gate Fault Interrupt	Commoned and connected to PDPINT*, which when unmasked and activated, immediately disables the PWM outputs (TMS320F4240 Processor). Response time is < 2μsec after fault detection, essentially limited by gate driver optocoupler transition time Fault status indicated by individual LEDs
Max IGBT Gate Current	Standard: 2A peak Enhanced: 6-8A peak (approximately)
PCB Connections	4 pin plug-in PCB Mounting Terminal Block, with Collector, Gate and Emitter connections (**X37** – **X44**)
Plug-in Interface to header	**X27** (which corresponds to J7 on the CS-MiniDSP)

2.6.2 TTL-Level Gate Drive Output

Definition	8 PWM Outputs
PWM Outputs	TTL Level – direct from Plug-In interface on **X27**
PWM Outputs from DSP Controller	8 PWM outputs consist of – 3 independent pairs (6 outputs) with programmable deadbands 2 independent compares (2 outputs) generated by the simple compare units – without deadband generation
PCB Connections	A 16-way IDC connector, providing 8 PWM outputs, interleaved with ground signals, **X31**
Plug-in Interface to header	**X27** (which corresponds to J7 on the CS-MiniDSP)

2.7 Communications Interface

2.7.1 RS-232 Interface

Definition	RS-232 connection, providing two pin serial communications for interface to a standard PC serial port
Isolation	1kV
Compatibility	Links provided to enable the board to be configured as a DTE or a DCE (**LK1**). Default is configuration as a DCE
PCB Connections	10-way IDC connector, with pin outs to suit standard PC 9 pin serial port (**X1**)
Plug-in Interface to header	**X17** (which corresponds to J5 on the CS-MiniDSP)

2.7.2 High Speed Serial Peripheral Interface

Definition	Half duplex synchronous clocked serial peripheral interface. Capable of operating in Master or Slave mode (software selected)
Compatibility	Compatible with the TMS320F2xx SPI module
PCB Connection	5-way Molex connector (**X11**)
Plug-in Interface to header	**X19** (which corresponds to J9 on the CS-MiniDSP)

2.8 General

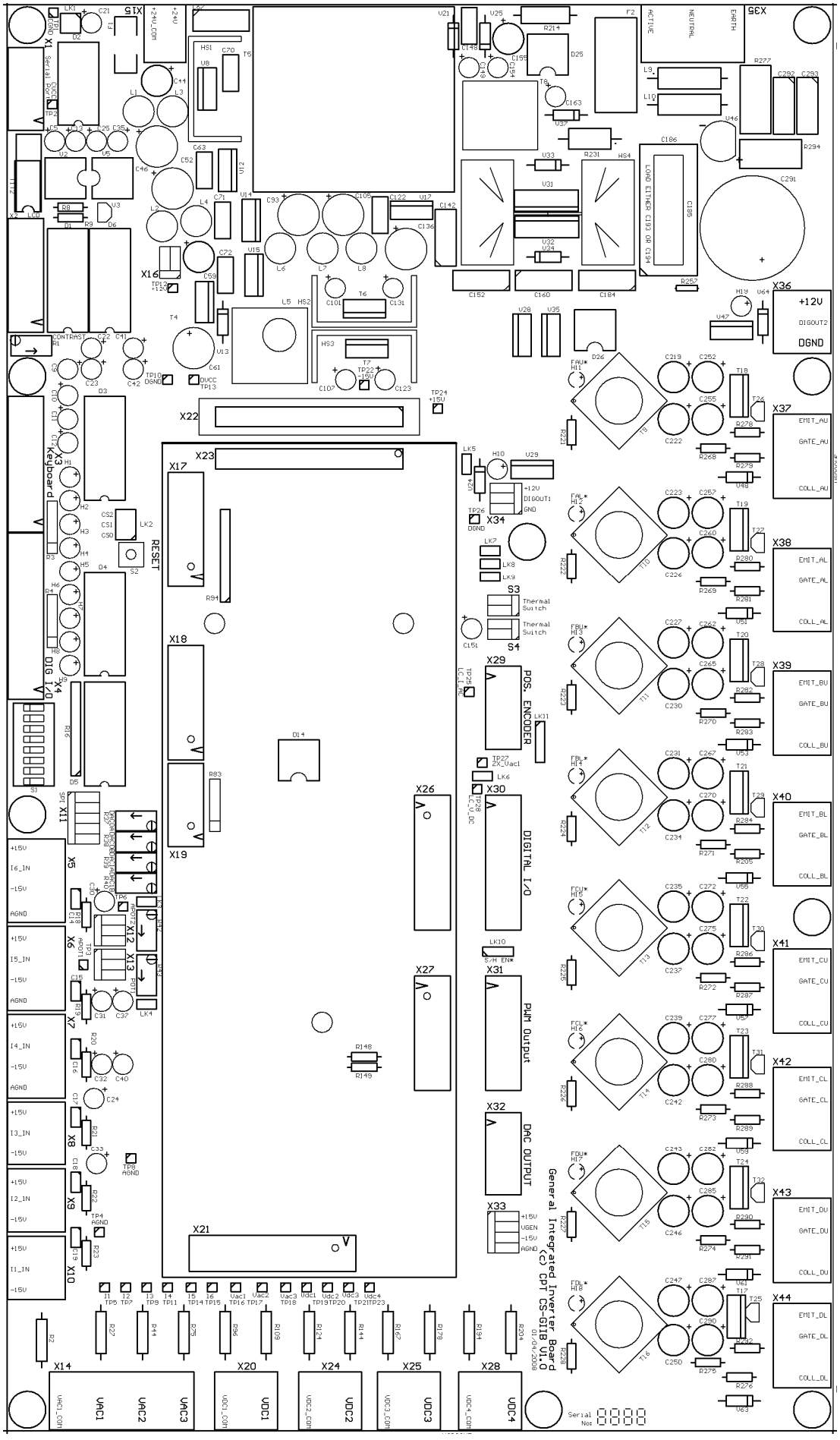
Physical Dimensions	L: 345mm
	W: 200mm
	H: 50mm approx.
Mounting Arrangement	10 off 4.5 mm holes spaced in a grid across the PCB (see Appendix B)
Environmental	0 – 50°C ambient operating temperature 5% - 95% non condensing humidity

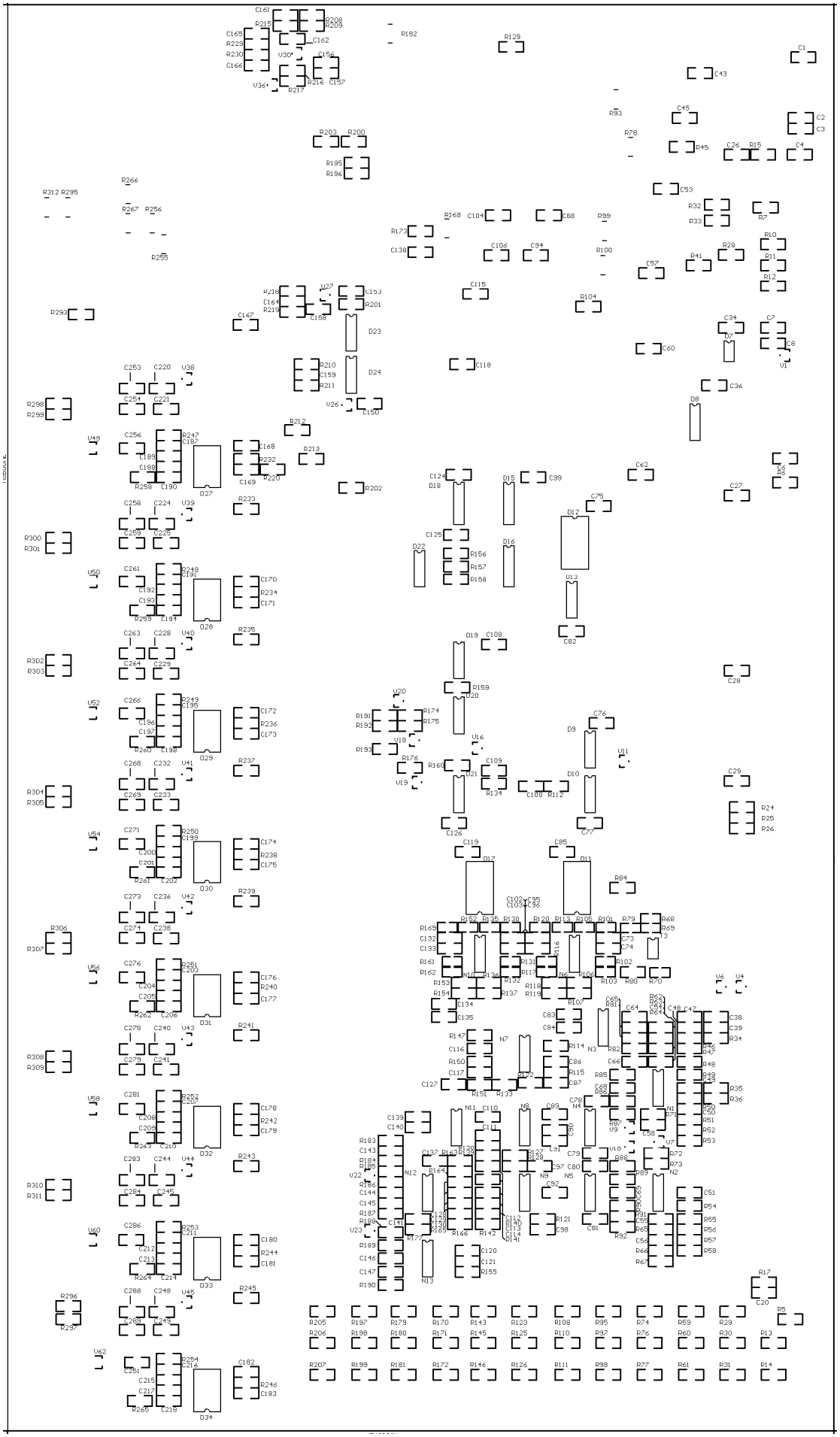
2.9 Power Supply

Input Voltage Range	90Vac – 270Vac (130Vdc – 370Vdc)
Standalone Input Current	**30**-**80** mA
Max Input Power	Approx. **36**W 2A Slow Blow Fuse Protected
Supplies Generated on-card	+12V Digital from which the +5V Digital is generated using a regulator
	±15V for Analog circuitry
	+24V Unregulated field supply - 1A total
	+17V/-12V Gate Drive Supply
Input Power Connector	3 pin plug-in PCB Mounting Terminal Block: Active, Neutral, EARTH (**X35**)
Output Power Connectors	2 pin plug-in PCB Mounting Terminal Block: +24V, GND_24V (**X15**) 2 pin Molex connector: +12V, DGND (**X16**)

Appendices

Appendix A Component Layout





Appendix B Mechanical Layout